

Structure : Silicon Monolithic Integrated Circuit
 Type : BU5963AS
 Product Series : On-Screen Display IC for VTR (NTSC format)
 Package Outlines : See Fig-1. (Plastic mold)
 Block Diagram : See Fig-2
 Functions :

MASTER

- Characters set by micro controller are superimposed with composite video signal which is input through VIDEOIN. (7 colors are settable for each character).
- Built-in SYNC SEP circuit. It separates SYNC signal from the composite video signal which has been input through VIDEOIN.
- Built-in APC circuit. It phases locks the color burst from input composite video signal and 3.58MHz frequency which comes from internal oscillator.
- Built-in AFC circuit which composes f_H of composite video signal from VIDEOIN and internal timing generator (f_H =Horizontal synchronizing frequency).
- The number of character dots is 12×18 . Up to 128 characters are stored in the built-in ROM.
- Up to 24×10 characters are able to display by the built-in RAM.
- Settable 4×4 character size and 64 H/V display starting position.
- Available to set from 8 kinds of display image which can be displayed in 8 different colors and also blinked.
- The BU2801S is operated only by 16bits serial interface from micro controller

Operating supply voltage 4.5 ~ 5.5 V

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	7	V
Operating input range	V_{IN}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Power dissipation	P_d	500	mW
Operating temp. range	T_{opr}	$-20 \sim +70$	$^\circ\text{C}$
Storage temp. range	T_{stg}	$-55 \sim +125$	$^\circ\text{C}$

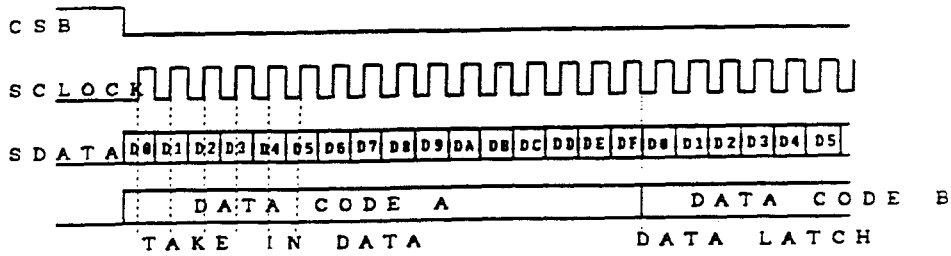
Design <i>Y. Ghimist</i>	Check <i>Yo Sawamura</i>	Approval <i>X. Kawakawa</i>	Date	8/SEP/94	Specification	Rev. A
			ROHM CO., LTD.		Specification No.	TSZ02201-BU5963AS-1-2

Electrical Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$)

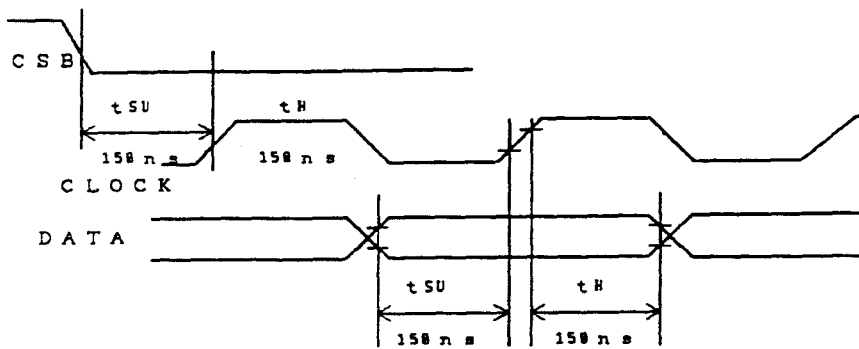
Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
Circuit current	IDD	7	35	45	mA	X0 stop mode
< LOGIC >						
Hysteresis input threshold	VHYSIN	1.5	-	3.5	V	HYS term.
Input current	IIN	-	0	1	μA	HYS term.
Output "L" voltage	VOL	-	0.3	1.0	V	LOUT term. IOU=1.0mA
Output "H" voltage	VOH	4.0	4.7	-	V	LOUT term. IOU=-1.0mA
Serial clock frequency	fMAX	-	-	2.5	MHz	SCLOCK
Data setup time	tSU	150	-	-	nS	SDATA/SCLOCK
Data hold time	tH	150	-	-	nS	SDATA/SCLOCK
Output "L" voltage	VOL	-	0.3	1.0	V	LOUT term. IOU=1.0mA
< VCXO >						
Bias voltage	VXOB	2.0	2.65	3.0	V	VCXOIN-VCXOOUT 1Mohmbias
Output "L" voltage	VXOL	-	0.3	1.0	V	VXOIN=VDD
Output "H" voltage	VXOH	4.0	4.7	-	V	VXOIN=GND
Oscillation frequency	FREF	14.31818			MHz	
< VIDEO SIGNAL >						
Composit input	VCIN	-	2	-	Vpp	Synctip-Whitepeak
Composit output	VCOU	1.5	2	2.5	Vpp	Synctip-Whitepeak B.Back
Cout "H" voltage	VCOH	4.0	4.5	-	V	COU trem. IOU=0.3mA
Cout "L" voltage	VCOL	-	0.5	1.0	V	COU term. IOU=0.3mA
< AFC >						
Amp input offset voltage	VOFF	-10	-2.5	+10	mV	Synctip-Whitepeak
Ampout "H" voltage	VAMPH	4.5	4.8	-	V	AMPOU trem. IOU=0.3mA
Ampout "L" voltage	VAMPL	-	0.2	0.8	V	AMPOU term. IOU=0.3mA
CLVout "H" voltage	VCLH	3.2	4.5	-	V	CLV trem. IOU=0.3mA
CLVout "L" voltage	VCLL	-	0.8	1.8	V	CLV term. IOU=0.3mA
COMP clamp level	VCOL	1.42	2.00	2.56	V	
< APC >						
POUT "H" voltage	VPDH	3.5	4.5	-	V	POU trem. IOU=1.0mA
POUT "L" voltage	VPDL	-	0.5	1.5	V	POU term. IOU=1.0mA
VIDEO clamp level	VPOL	2.10	2.00	1.50	V	

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Serial Data Timing



SDATA is received at the start of SCLOCK. Data is input each 16 CLOCK pulses.



* F c k (M A X) = 2 . 5 M H z

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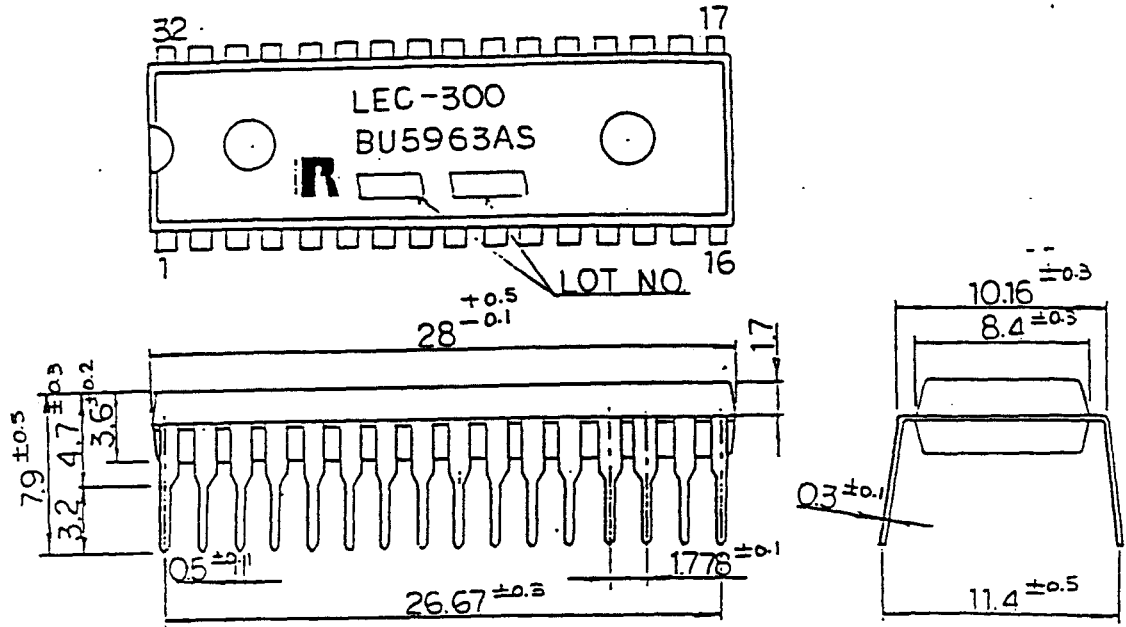


Fig-1 OUTLINE (Unit:mm)
(Plastic mold)

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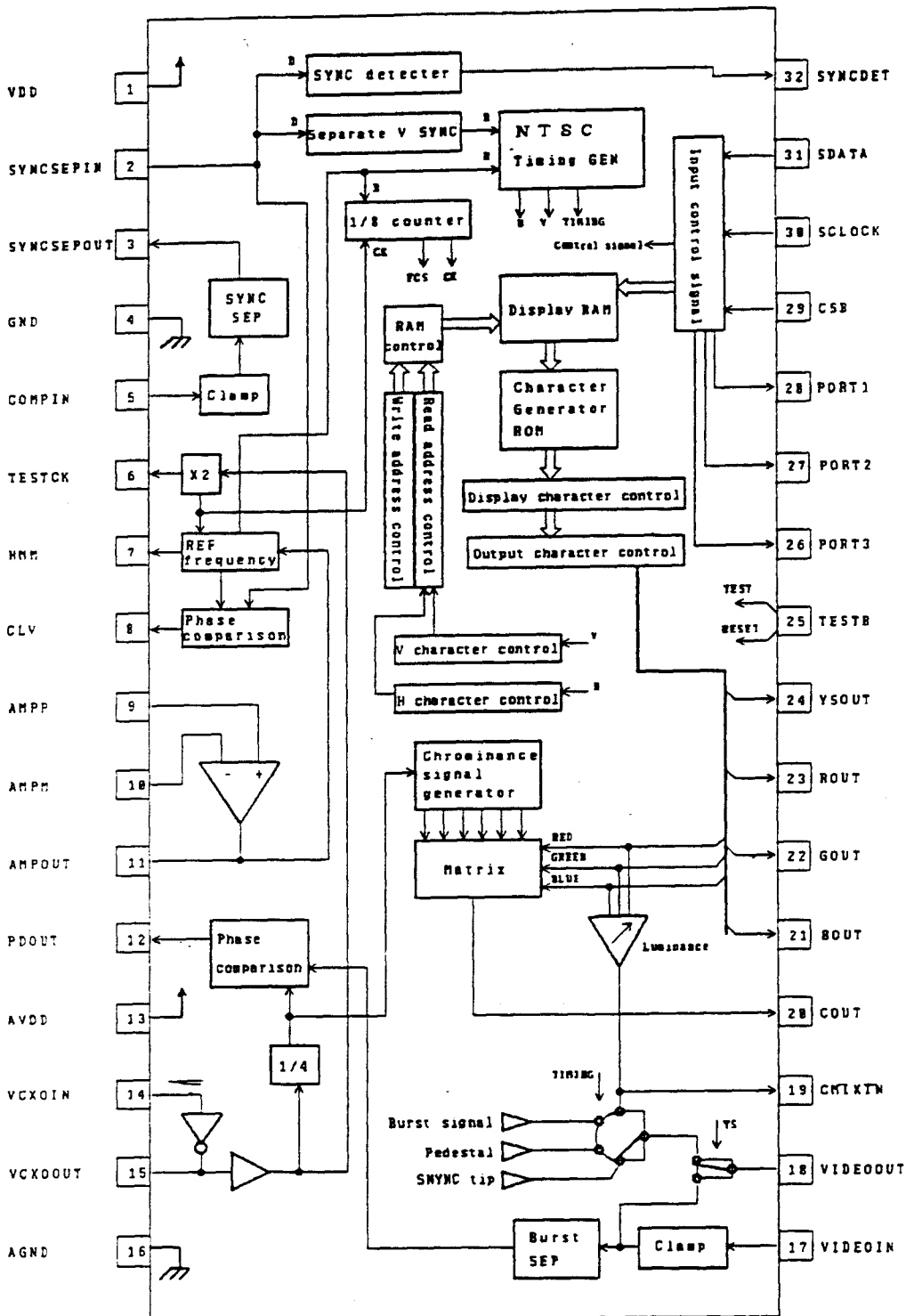


Fig-2 Block Diagram

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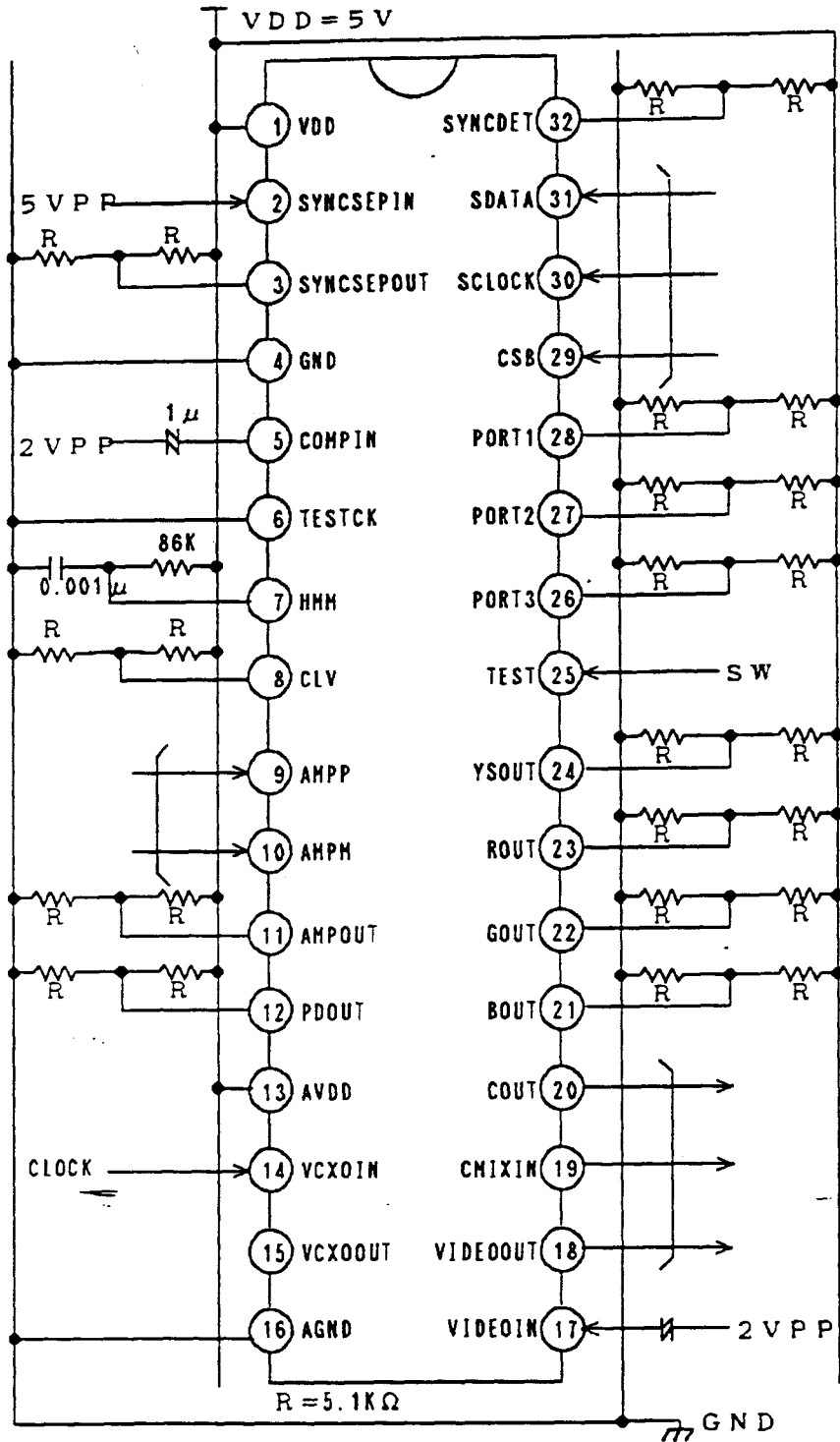


Fig-3 Measurement circuit

Date	8/SEP/94	Specification	
ROHM CO., LTD.		Specification No.	TSZ02201-BU5963AS-1-2

Terminal Function

Pin No	Terminal code	Function	I/O cell
1	VDD		
2	SYNCSEPIN	Input composite SYNC signal	AIO
3	SYNCSEPOUT	Output SYNC signal separated internally(Output CMOS)	LOUT
4	GND		
5	COMPIN	Input composite video signal	AIO
6	TESTCK	Terminal to connect capacitor for multiplication(X2)	AIO
7	HMM	Terminal to connect CR for AFC mono-multi	MMP
8	CLV	AFC control voltage	CLV
9	AMPP	Input AFC comparator (+)	AIO
10	AMPM	Input AFC comparator (-)	AIO
11	AMPOUT	Output AFC comparator	LOUT
12	PDOUT	Output APC control voltage	PDP
13	AVDD		
14	VCXOIN	Terminal for connecting crystal (14.31818MHz)	VCXO
15	VCXOOUT		
16	AGND		
17	VIDEOIN	Input composite video signal	AIO
18	VIDEOOUT	Output composite video signal with Superimposing	AIO
19	CMIXIN	Input chrominance signal for mixing with luminance signal. (output luminance signal)	AIO
20	COUT	Output chrominance signal	AIO
21	BOUT	RGB signals output (CMOS output)	LOUT
22	GOUT	Each RGB signal output has no relation to the status of YSOUT.	LOUT
23	ROUT		LOUT
24	YSOUT	Superimposing timing output. YSOUT depends on character data. However, YSOUT is low when composite video signal is passing through.	LOUT
25	TESTB	Terminal of power on reset and test H: Operation M: Test L: Reset	TIN
26	PORT3	Output control signal	LOUT
27	PORT2		LOUT
28	PORT1		LOUT
29	CSB	Serial data · Chip select input	HYS
30	SCLOCK	Serial data · Clock input	HYS
31	SDATA	Serial data · Data input	HYS
32	SYNCDET	Output SYNC detector L: exist H: not exist	LOUT

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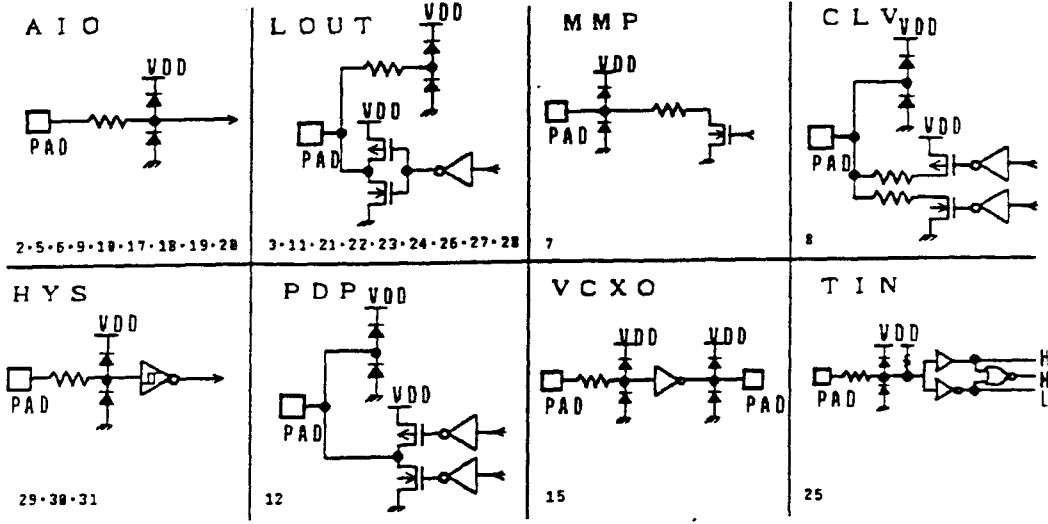


Fig-4 Circuit of terminal

Date	8/SEP/94	Specification
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Composition of Memory

Configuration of RAM for display and register for controlling display are composed of 16 bits. Address is available from 0 to 243. RAM address for display character data is from 0 to 239. Register for controlling display is from address 240 to 243. There are 2 kinds of data receiving modes, addressing mode and data mode.

Bit 13 switches-between each mode. When setting bit 13 for "0", data mode is applied. When setting bit 13 for "1", addressing mode is applied and address can be set at 8 bits (0-7 bit) from the bottom.

After setting an address, the first data is written in it, and after that, the address is increased for every additional data.

Construction of data

Bit	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A/D	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Addressing mode

Bit	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0

Data mode

Bit/ Add.	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SPC Super ON/OFF	B Character	G colors	R Blink	BLNK	O	CD6	CD5	CD4	CD3	CD2	CD1	CD0
239	0	SPC	B	G	R	BLNK	O	CD6	CD5	CD4	CD3	CD2	CD1	CD0
240	0	*	*	*	HS21	HS20	HS11	HS10	HCP5	HCP4	HCP3	HCP2	HCP1	HCP0
241	0	*	*	*	VS21	VS20	VS11	VS10	VCP5	VCP4	VCP3	VCP2	VCP1	VCP0
242	0	*	*	*	*	HB	HG	HR	SB	SG	SR	BB	BG	BR
243	0	POR3	POR2	POR1	HC1	HC0	BRB	BI	BCN1	BCN0	BFC	DP2	DP1	DPO

Note1: Whichever the mode is, please set bit 14 and 15 for "0". Note2: Mark* means undefined.

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Address 0~239

Register		Function
DC	SPC	Switch-over the character to be superimposed or output at RGB out. 1: Superimpose 2: RGB OUT: ϕ
DB	B	Display character color Blue
DA	G	Display character color Green
D9	R	Display character color Red
D8	BLNK	ON/OFF switch of reverse display. 1: ON 0: OFF
D7	Undefined	
D6	CD6	Character code (MSB)
D5	CD5	.
D4	CD4	.
D3	CD3	.
D2	CD2	.
D1	CD1	.
D0	CD0	(LSB)

Note: When all registers "R", "G" and "B" are "0", character isn't displayed in no relation with BLINK, SPC nor character code.

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Address 240

Register	status	Function
DC	0	
DB	0	
DA	0	
D9	HS21	Set horizontal character size. (from line to 10) 1TC is about 140ns
	0	
	1	
D8	HS20	
	0	
	1	
D7	HS11	Set horizontal character size. (the first line) 1TC is about 140ns
	0	
	1	
D6	HS10	
	0	
	1	
D5	HCP5	Starting position of horizontal character. Set starting position of display horizontal character.
	0	
	1	
D4	HCP4	Starting display position = $T_c \times \sum_{n=0}^5 2^n \cdot HCP_n$. Tc is about 140ns
	0	
	1	
D3	HCP3	
	0	
	1	
D2	HCP2	
	0	
	1	
D1	HCP1	
	0	
	1	
D0	HCP0	
	0	
	1	

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Address 241

Register	Status	Function													
DC	0														
DB	0														
DA	0														
D9	VS21	Set vertical character size.(line 2 to 10) *H* means horizontal synchronizing time.													
	0		<table border="1"> <tr> <td></td> <td colspan="2">VS20</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> </tr> <tr> <td>VS21</td> <td>0</td> <td>1H/dot</td> <td>2H/dot</td> </tr> <tr> <td></td> <td>1</td> <td>3H/dot</td> <td>4H/dot</td> </tr> </table>		VS20			0	1	VS21	0	1H/dot	2H/dot		1
	VS20														
	0	1													
VS21	0	1H/dot	2H/dot												
	1	3H/dot	4H/dot												
D8	VS20	*H* means horizontal synchronizing time.													
	0		<table border="1"> <tr> <td></td> <td colspan="2">VS10</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> </tr> <tr> <td>VS11</td> <td>0</td> <td>1H/dot</td> <td>2H/dot</td> </tr> <tr> <td></td> <td>1</td> <td>3H/dot</td> <td>4H/dot</td> </tr> </table>		VS10			0	1	VS11	0	1H/dot	2H/dot		1
	VS10														
	0	1													
VS11	0	1H/dot	2H/dot												
	1	3H/dot	4H/dot												
D7	VS11	Set vertical character size. (the first line) *H* means horizontal synchronizing time.													
	0		<table border="1"> <tr> <td></td> <td colspan="2">VS10</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> </tr> <tr> <td>VS11</td> <td>0</td> <td>1H/dot</td> <td>2H/dot</td> </tr> <tr> <td></td> <td>1</td> <td>3H/dot</td> <td>4H/dot</td> </tr> </table>		VS10			0	1	VS11	0	1H/dot	2H/dot		1
	VS10														
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VS11	0	1H/dot	2H/dot												
	1	3H/dot	4H/dot												
D6	VS10	*H* means horizontal synchronizing time.													
	0		<table border="1"> <tr> <td></td> <td colspan="2">VS10</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> </tr> <tr> <td>VS11</td> <td>0</td> <td>1H/dot</td> <td>2H/dot</td> </tr> <tr> <td></td> <td>1</td> <td>3H/dot</td> <td>4H/dot</td> </tr> </table>		VS10			0	1	VS11	0	1H/dot	2H/dot		1
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D5	VCP5	Starting position of vertical character. Set starting position of display vertical character.													
	0														
D4	VCP4	Starting display position = $H \times \sum_{n=0}^5 2^n \cdot VCP_n$ *H* means horizontal synchronizing time.													
	0														
D3	VCP3	*H* means horizontal synchronizing time.													
	0														
D2	VCP2	*H* means horizontal synchronizing time.													
	0														
D1	VCP1	*H* means horizontal synchronizing time.													
	0														
D0	VCP0	*H* means horizontal synchronizing time.													
	0														

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Address 242

	Register	Status	Function	
DC		0		
DB		0		
DA		0		
D9		0		
D8	HB	0	Setting outline color	Blue
		1		
D7	HG	0	Setting outline color	Green
		1		
D6	HR	0	Setting outline color	Red
		1		
D5	SB	0	Character size color	Blue
		1		
D4	SG	0	Character size color	Green
		1		
D3	SR	0	Character size color	Red
		1		
D2	BB	0	Background color	Blue
		1		
D1	BG	0	Background color	Green
		1		
D0	BR	0	Background color	Red
		1		

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Address 243

Register	Status	Function																																				
DC	PORT3	0 26PIN "L" output																																				
		1 "H"																																				
DB	PORT2	0 27PIN "L" output																																				
		1 "H"																																				
DA	PORT1	0 28PIN "L" output																																				
		1 "H"																																				
D9	HC1	0 Control display of outline and character size HCO=0 HC1=0; Normal character HCO=1 HC1=0; Outline																																				
		1																																				
D8	HCO	0 HCO=0 HC1=1; Character size																																				
		1 HCO=1 HC1=1; Character size and outline																																				
D7	BRB	0 Control display mode to be reversed or non-display of characters which have been set blinking. "1": Normal "0": reversed																																				
		1																																				
D6	BI	0 When blinking is off, set display mode of characters which have been set blinking. "1": Normal "0": reversed or non-display																																				
		1																																				
D5	BCN1	Duty control of blinking/reverse display	<table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="2">BCN0</th> </tr> <tr> <th colspan="2"></th> <th>0</th> <th>1</th> </tr> </thead> <tbody> <tr> <th rowspan="2">BCN1</th> <th>0</th> <td>Blinking OFF</td> <td>duty25%</td> </tr> <tr> <th>1</th> <td>Duty50%</td> <td>duty75%</td> </tr> </tbody> </table>			BCN0				0	1	BCN1	0	Blinking OFF	duty25%	1	Duty50%	duty75%																				
					BCN0																																	
		0	1																																			
BCN1	0	Blinking OFF	duty25%																																			
	1	Duty50%	duty75%																																			
D4	BCN0	0																																				
		1																																				
D3	BFC	0 Setting of blinking frequency. "1": 64 frequency dividing of vertical synchronizing time. "0": 32 frequency dividing.																																				
		1																																				
D2	DP2	<table border="1"> <thead> <tr> <th>DP0</th> <th>DP1</th> <th>DP2</th> <th>OUTPUT MODE</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Superimposing</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Superimposing</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Superimposing</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Superimposing</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Input picture signal</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Superimposing</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Mono-color character (Interlace)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Mono-color character (Non-interlace)</td> </tr> </tbody> </table>	DP0	DP1	DP2	OUTPUT MODE	1	0	0	Superimposing	1	0	1	Superimposing	1	1	0	Superimposing	1	1	1	Superimposing	0	0	0	Input picture signal	0	0	1	Superimposing	0	1	0	Mono-color character (Interlace)	0	1	1	Mono-color character (Non-interlace)
		DP0	DP1	DP2	OUTPUT MODE																																	
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@VIDEOOUT

Relation of VIDEOOUT Signal and DP0, DP1, DP2 SW

DP0	DP1	DP2	OUTPUT MODE
1	0	0	SUPERIMPOSE
1	0	1	SUPERIMPOSE
1	1	0	SUPERIMPOSE
1	1	1	SUPERIMPOSE
0	0	0	INPUT VIDEO Signal
0	0	1	SUPERIMPOSE
0	1	0	BLUEBACK Signal (INTERLACE)
0	1	1	BLUEBACK Signal (NONINTERLACE)

@YSOUT

YSOUT is synchronized with character data on SUPERIMPOSE MODE or BLUEBACK MODE.
But, on INPUT VIDEO Signal MODE, is fixed LOW level.

@ROUT/GOUT/BOUT

RGBOUT is normally out whenever YSOUT is out or not.

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On the TV screen, display position and RAM address are as follows.
 (Address 00_H starts from upper left side)

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47
48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77
78	79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	AA	AB	AC	AD	AE	AF	AG	A7
AB	A9	AA	AB	AC	AD	AE	AF	80	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
CB	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7
DB	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF




Fig-5 Composition of the TV Screen

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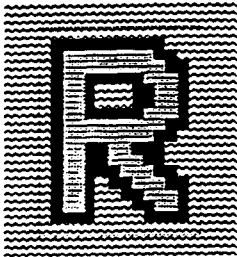
Display Image (non-reversed display)





Normal display (HC0=HC1=0)



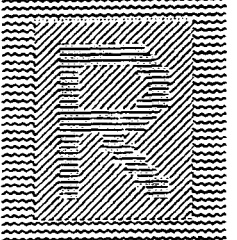
-  Character size (12x18dot)
-  Decided by R. G. B. of each character
-  Picture, or mono-color background
Decided by BR, BG, BB





Outline display (HC0=1, HC1=0)



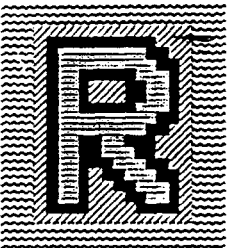
-  Character size (12x18dot)
-  Decided by R. G. B. of each color.
-  Outline color is decided by HR, HG, HB
-  Picture, or mono-color background
Decided by BR, BG, BB






Character size display (HC0=0, HC1=1)



-  Character size (12x18dot)
-  Decided by R. G. B. of each color
-  Decided by character size Color SR, SG, SB
-  Picture, or mono-color background
Decided by BR, BG, BB

Character size and outline display (HC0=HC1=1)

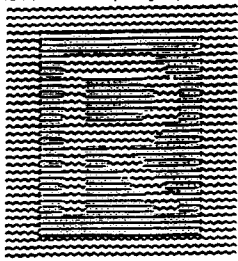





-  Character size (12x18dot)
-  Decided by R. G. B. of each character
-  Outline color is decided by HR, HG, HB
-  Decided by character size color SR, SG, SB
-  Picture, or mono-color background
Decided by BR, BG, BB

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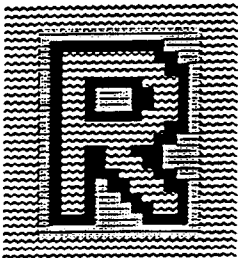
Display Image (reversed display)





Normal display (HC0=HC1=0)



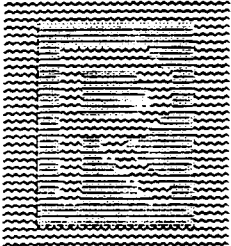
-  Character size (12×18dot)
-  Decided by R, G, B. of each character
-  Picture, or mono-color background
Decided by BR, BG, BB





Outline display (HC0=1, HC1=0)



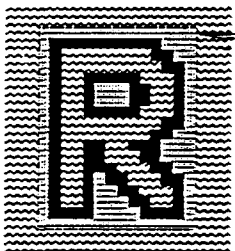
-  Character size (12×18dot)
-  Decided by R, G, B. of each color
-  Outline color is decided by HR, HG, HB
-  Picture, or mono-color background
Decided by BR, BG, BB






Character size display (HC0=0, HC1=1)



-  Character size (12×18dot)
-  Decided by R, G, B. of each character
-  Decided by character size color SR, SG, SB
-  Picture, or mono-color background
Decided by BR, BG, BB

Character size and outline display (HC0=HC1=1)



-  Character size (12×18dot)
-  Decided by R, G, B. of each character
-  Outline color is decided by HR, HG, HB
-  Decided by character size color SR, SG, SB
-  Picture, or mono-color background
Decided by BR, BG, BB

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Outline Data

Outline characters are generated in dots which have no character data but character data exists in adjoining the dot.

Outline can't be generated;

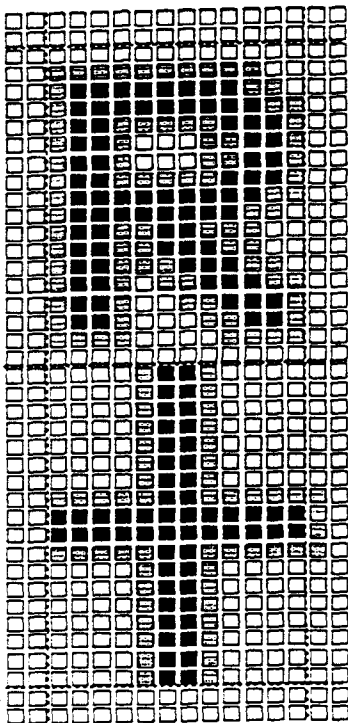
- above the character data which is on the first rank.
- under the character data which is on the 18th rank.
- left to the character data which is on the first file.

When character is on the 12th file, outline data occurs on the right side of the character.

However, it does not appear on the screen if the next character data is off.

A character is defined as "off" when;

1. character color setting is R=G=B=0.
2. character setting is SPC=0.
3. blinking is set and blinkin is on.

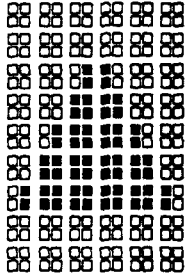


- Blank
- Character data
- Outline data
- Character size

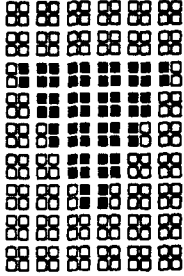
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キャラクタデータ 1

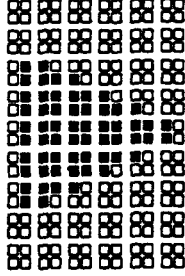
0 0



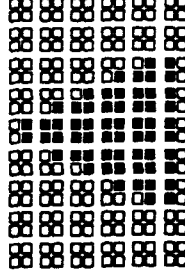
0 1



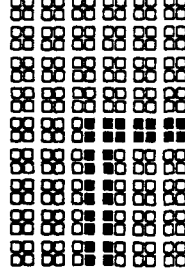
0 2



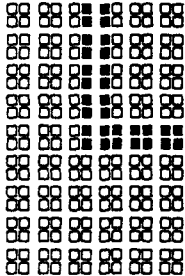
0 3



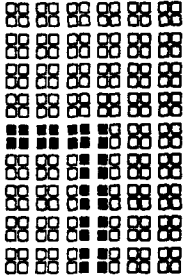
0 4



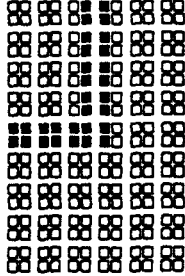
0 5



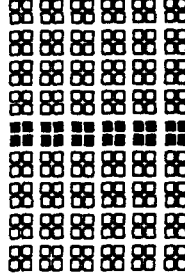
0 6



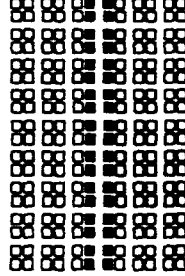
0 7



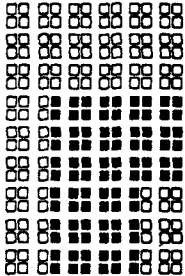
0 8



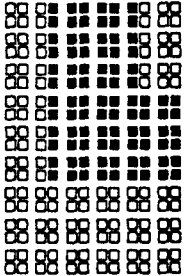
0 9



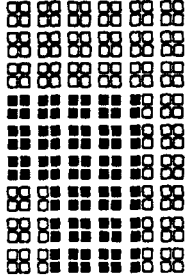
0 A



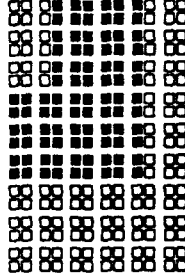
0 B



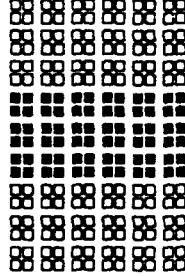
0 C



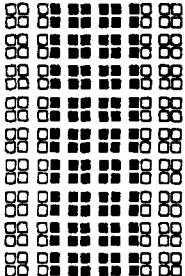
0 D



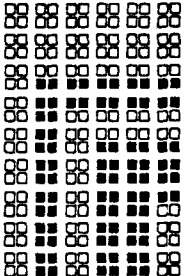
0 E



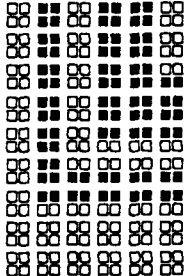
0 F



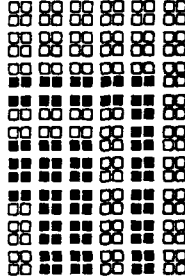
1 0



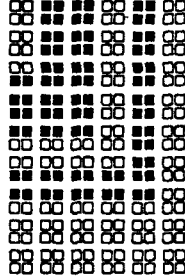
1 1



1 2

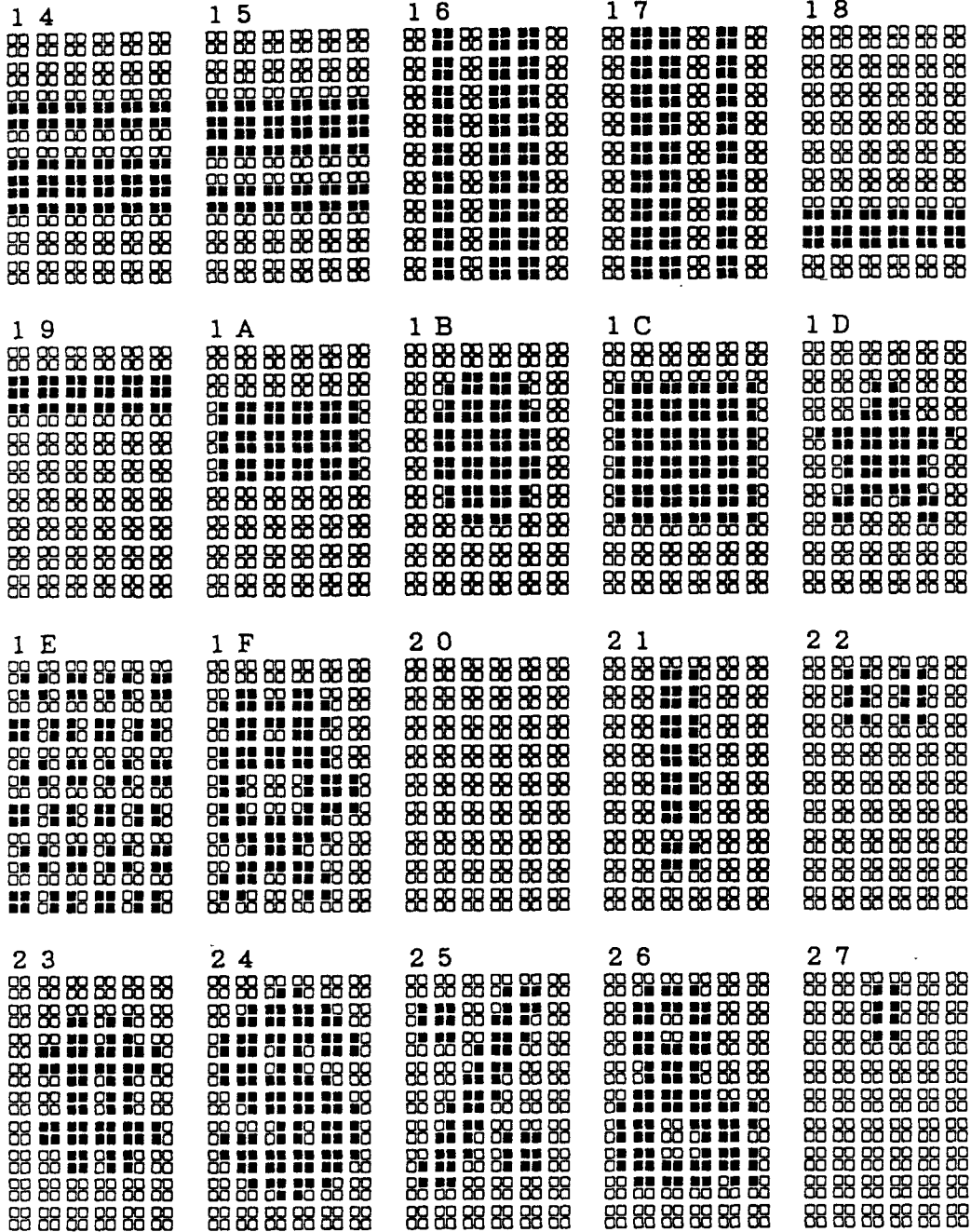


1 3



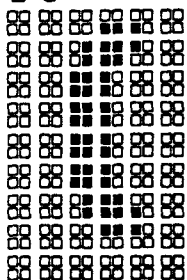
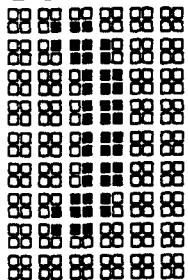
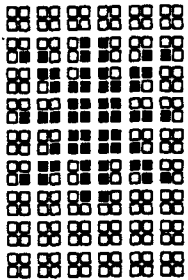
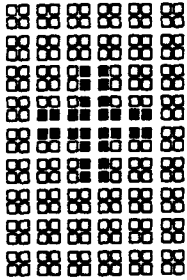
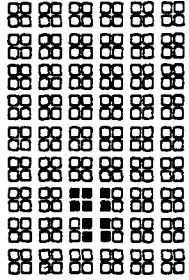
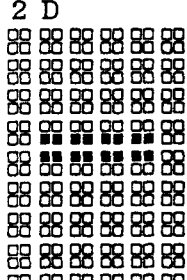
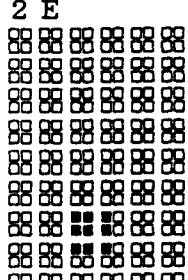
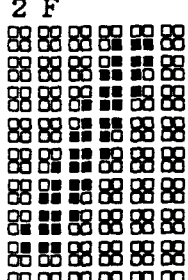
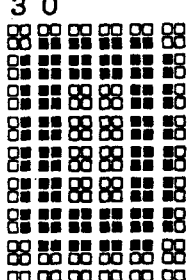
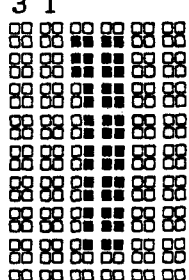
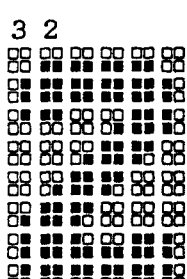
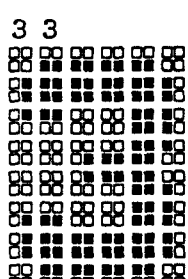
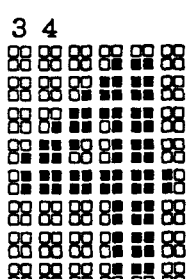
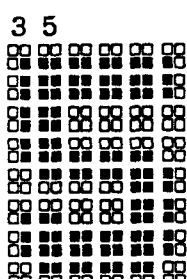
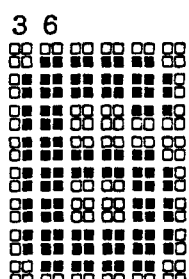
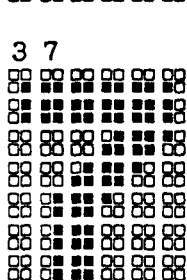
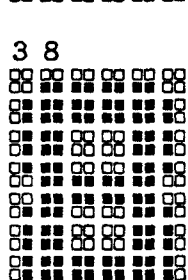
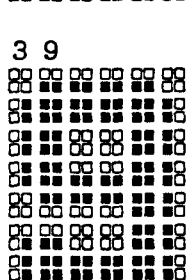
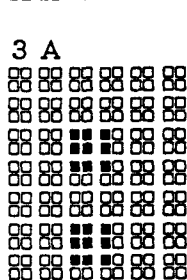
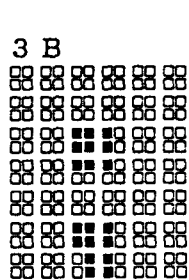
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キャラクタデータ 2



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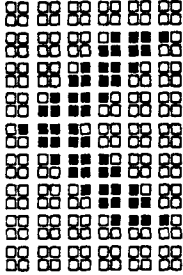
キャラクターデータ 3

2 8 	2 9 	2 A 	2 B 	2 C 
2 D 	2 E 	2 F 	3 0 	3 1 
3 2 	3 3 	3 4 	3 5 	3 6 
3 7 	3 8 	3 9 	3 A 	3 B 

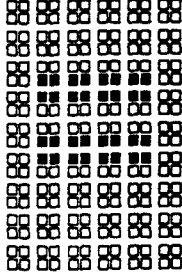
Date 3/10/18	Specification
ROHM CO., LTD.	Specification No.

キャラクターデータ 4

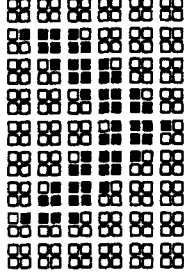
3 C



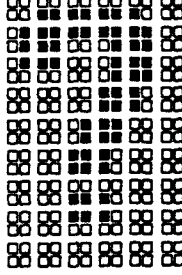
3 D



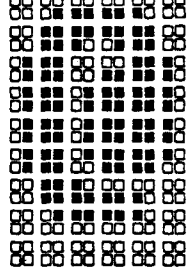
3 E



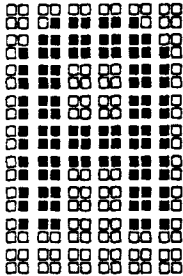
3 F



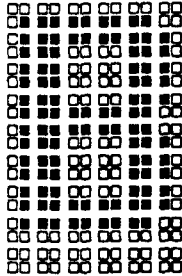
4 0



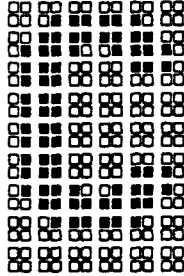
4 1



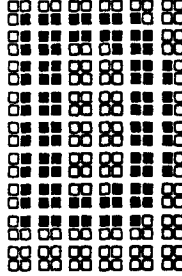
4 2



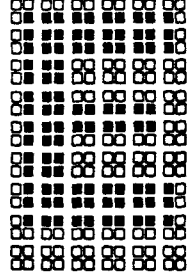
4 3



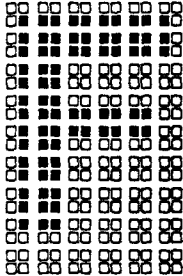
4 4



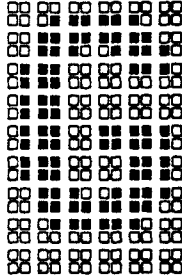
4 5



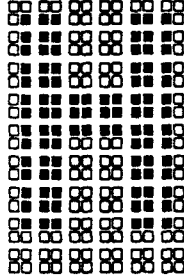
4 6



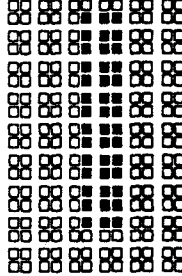
4 7



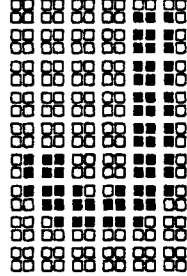
4 8



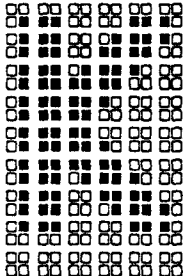
4 9



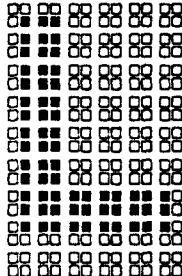
4 A



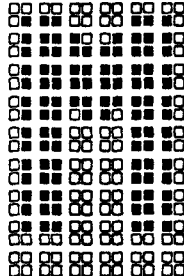
4 B



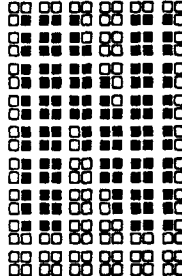
4 C



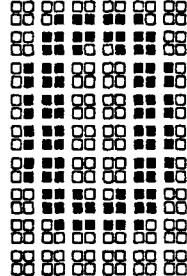
4 D



4 E



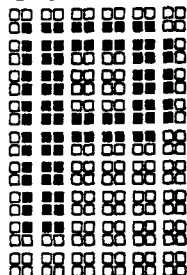
4 F



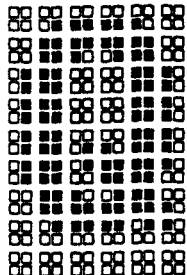
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キャラクタデータ 5

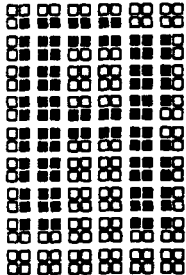
5 0



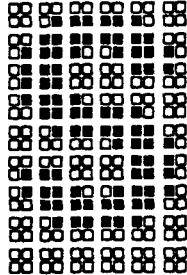
5 1



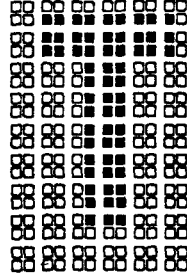
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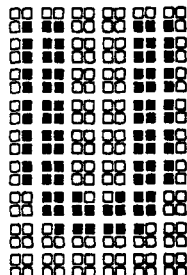
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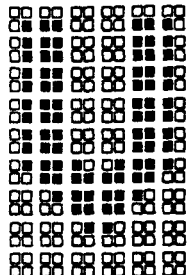
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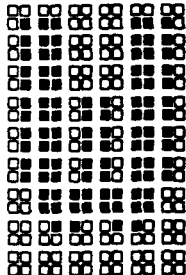
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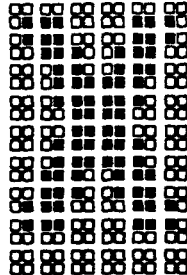
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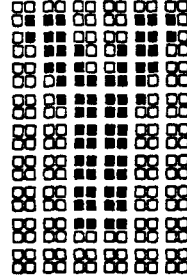
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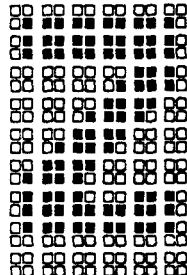
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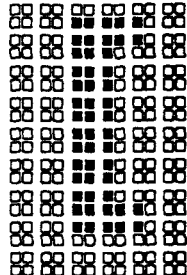
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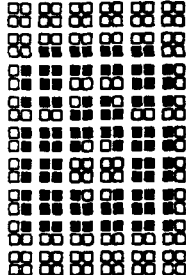
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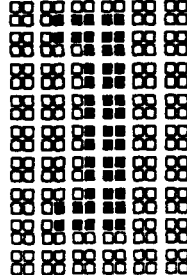
5 B



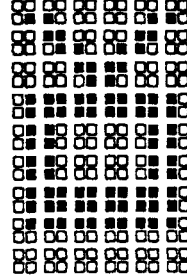
5 C



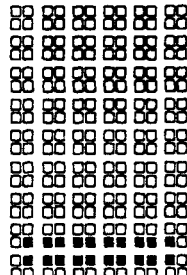
5 D



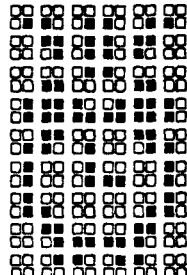
5 E



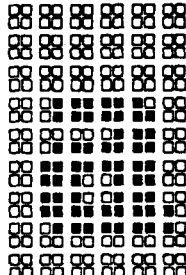
5 F



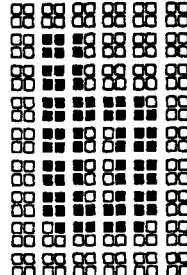
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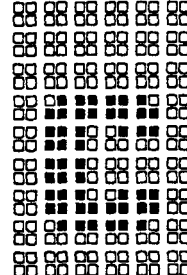
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6 2



6 3

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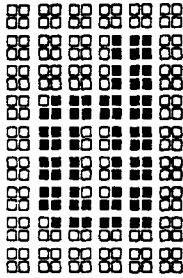
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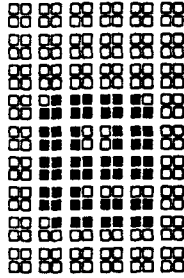
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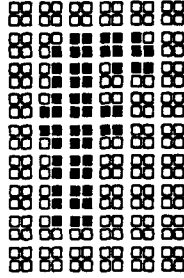
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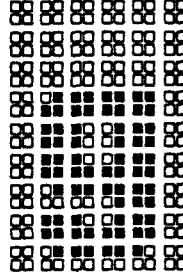
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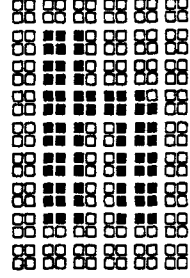
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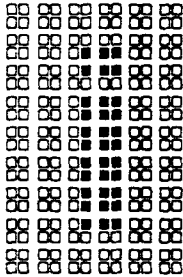
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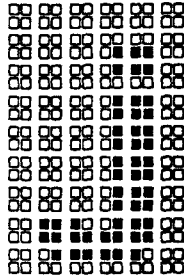
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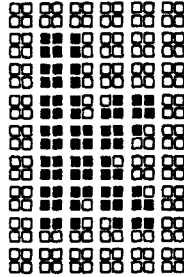
6 9



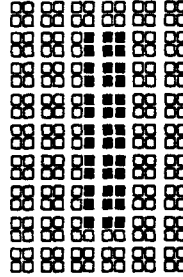
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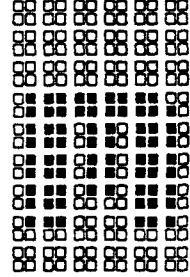
6 B



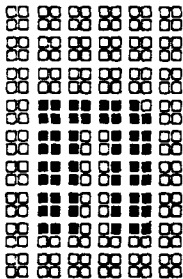
6 C



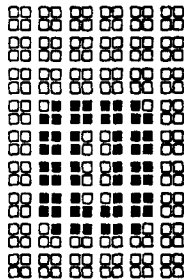
6 D



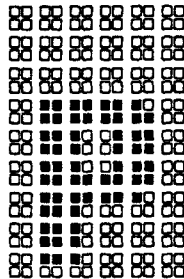
6 E



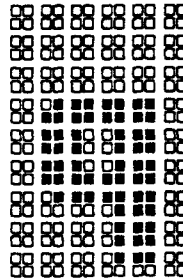
6 F



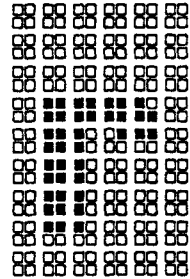
7 0



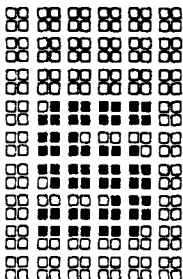
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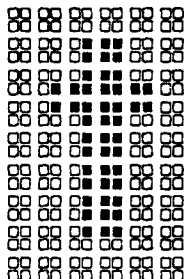
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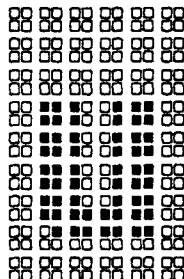
7 3



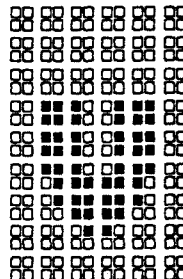
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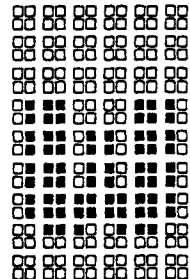
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7 6



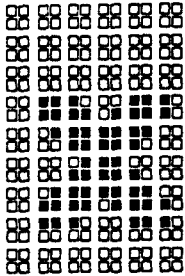
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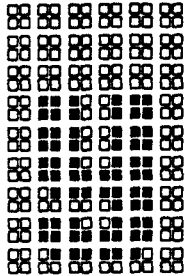
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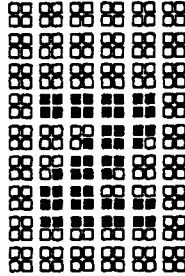
7 8



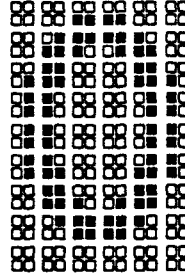
7 9



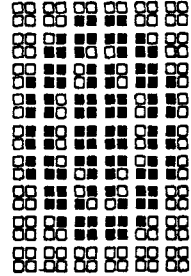
7 A



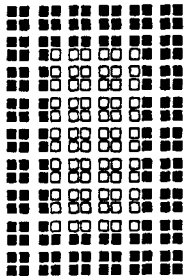
7 B



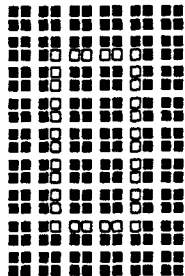
7 C



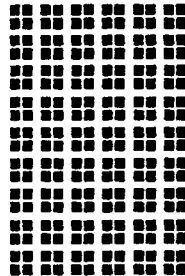
7 D



7 E



7 F



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